

Parallel VID Communication

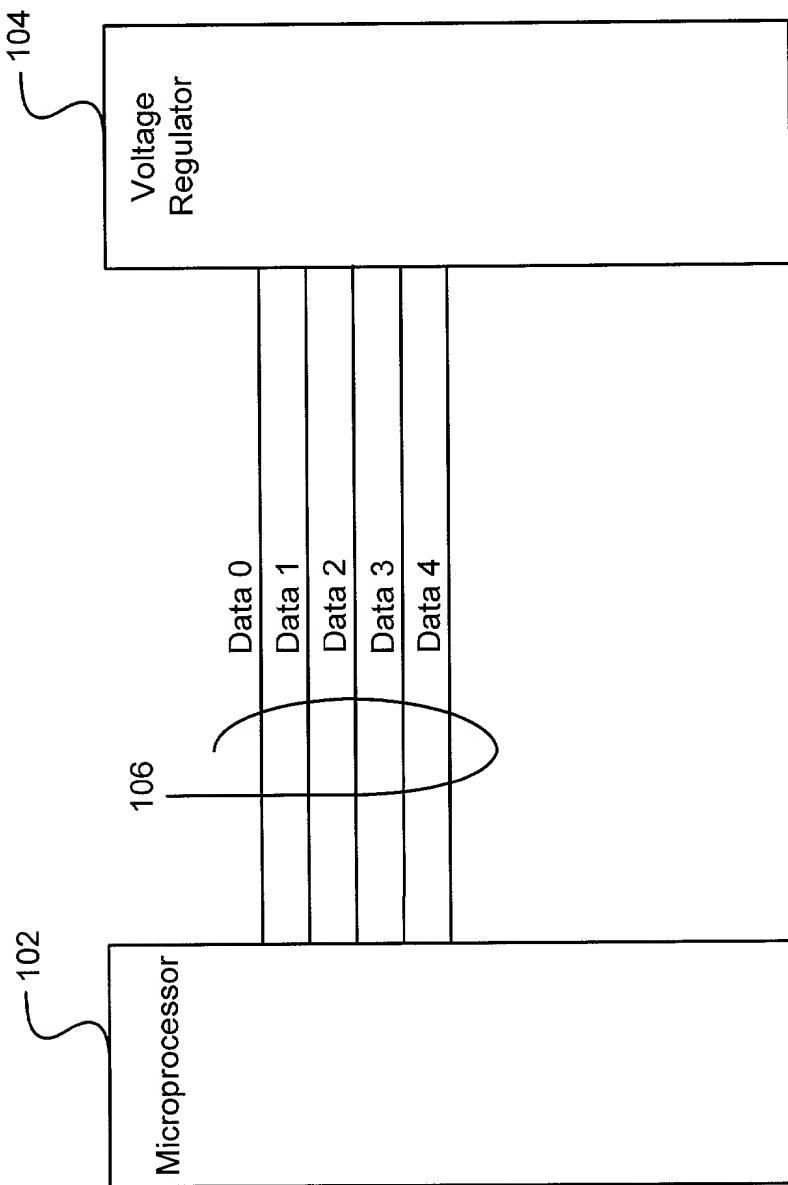
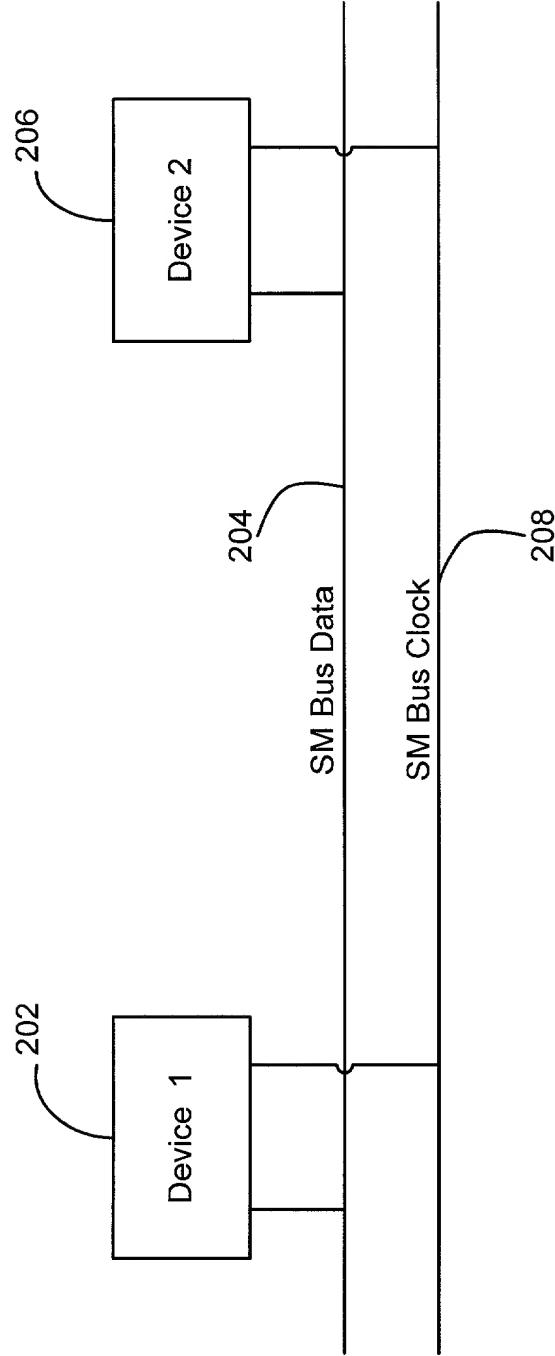


Fig. 1
Prior Art

SM Bus



**Fig. 2
Prior Art**

Serial VID Interface

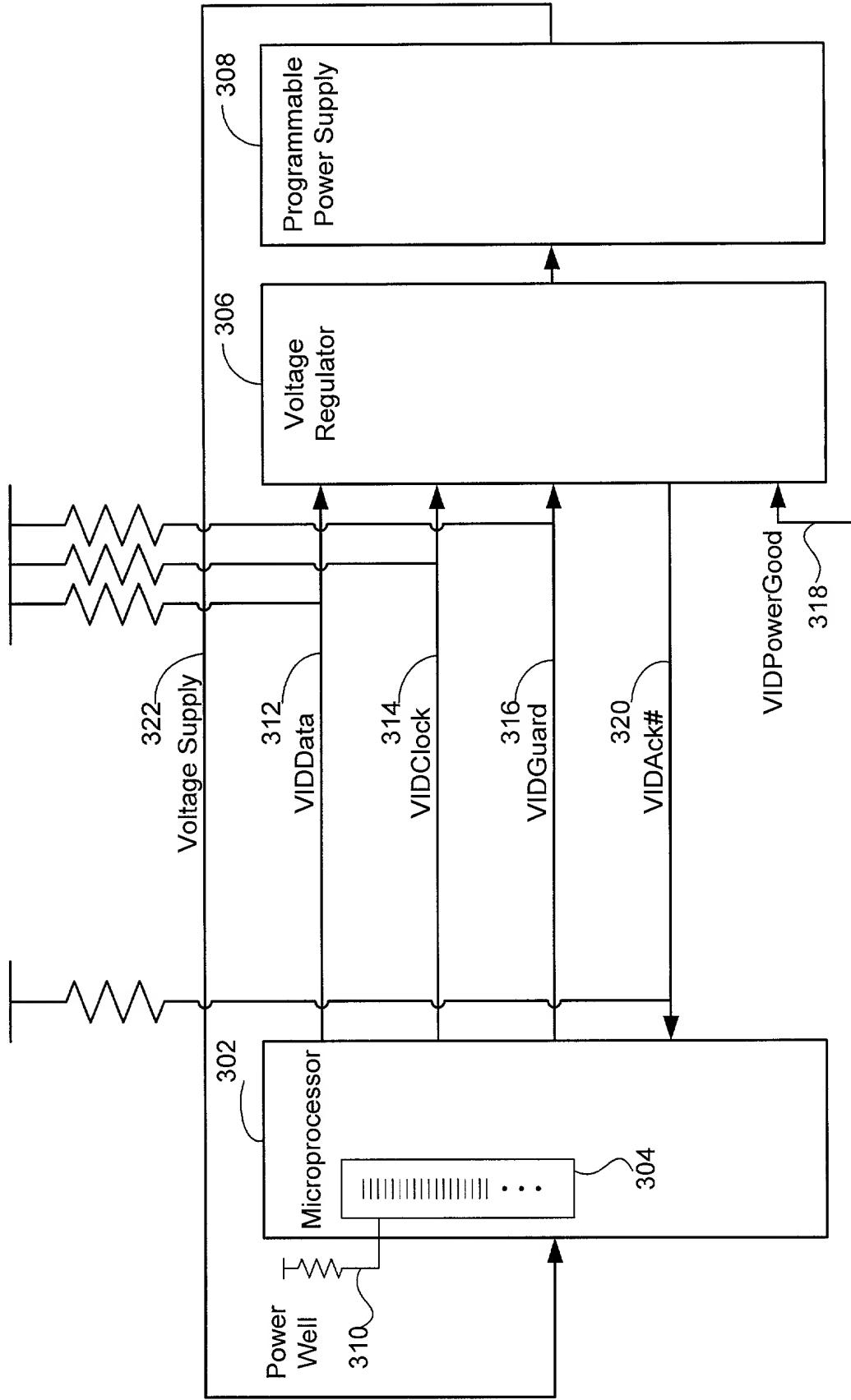


Fig. 3

VIDDData and VIDGuard Timing

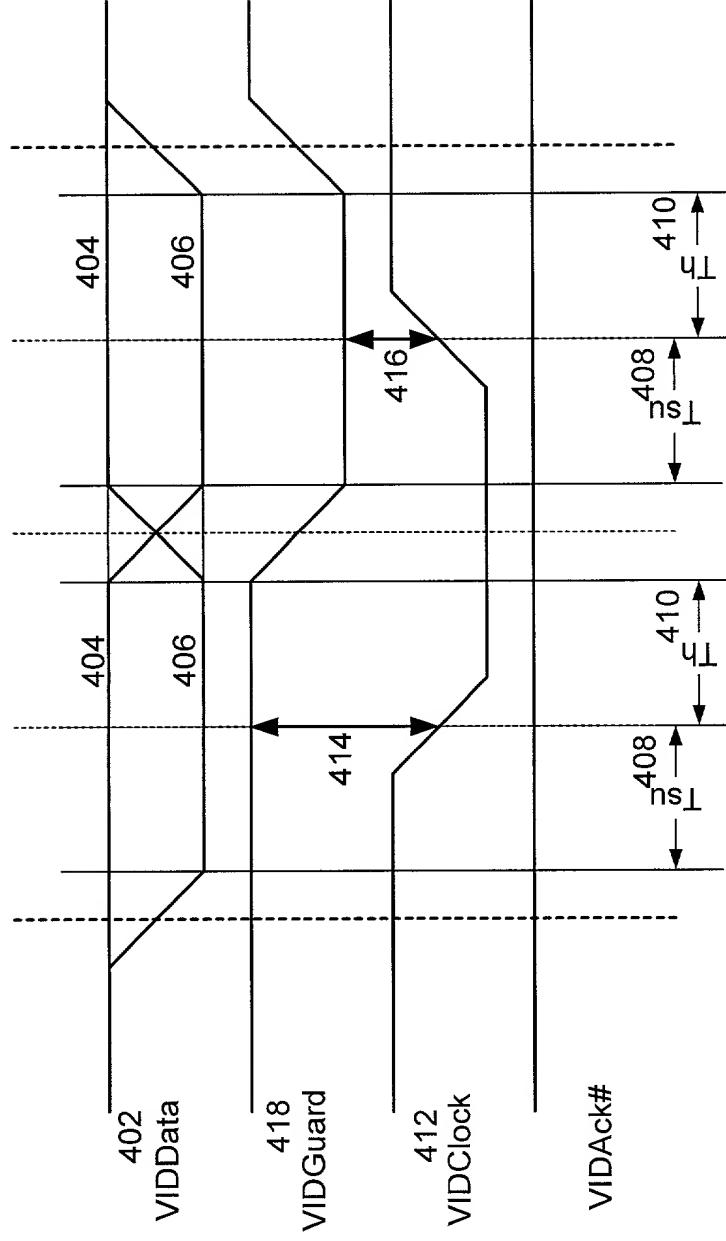


Fig. 4

VIDAck# Timing

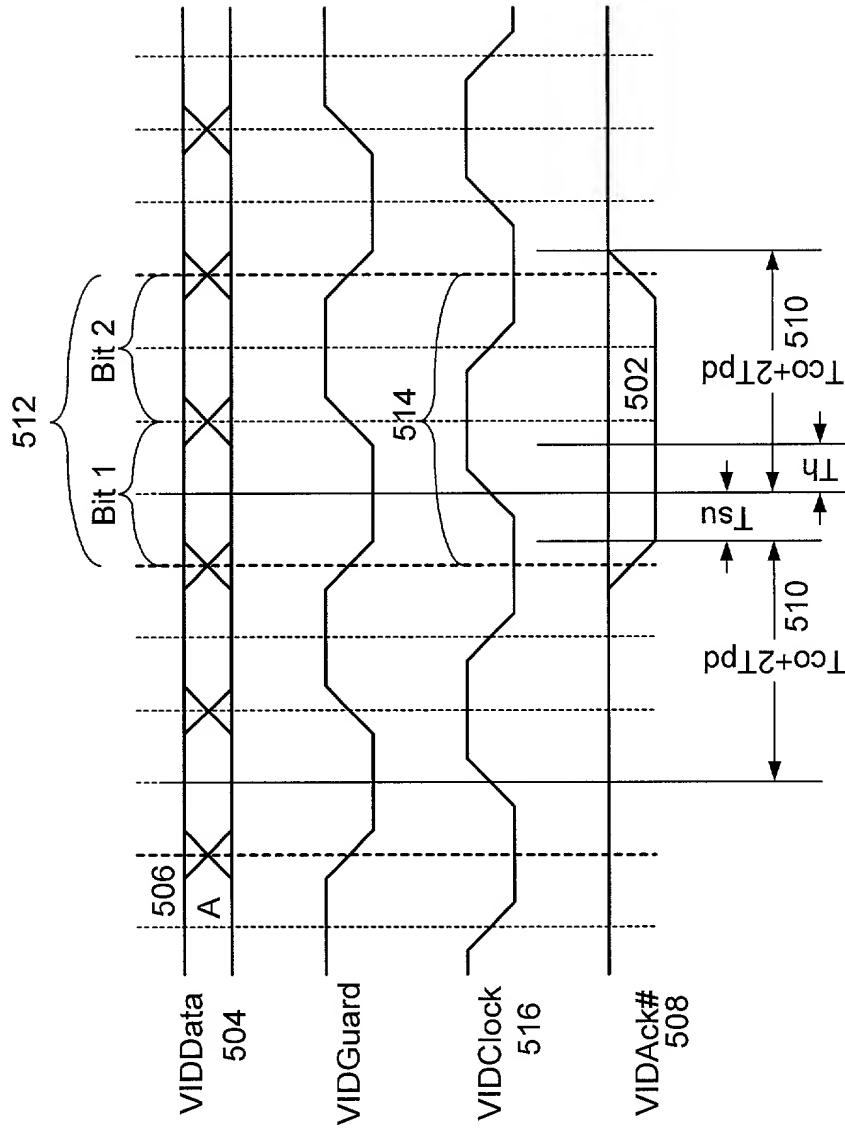
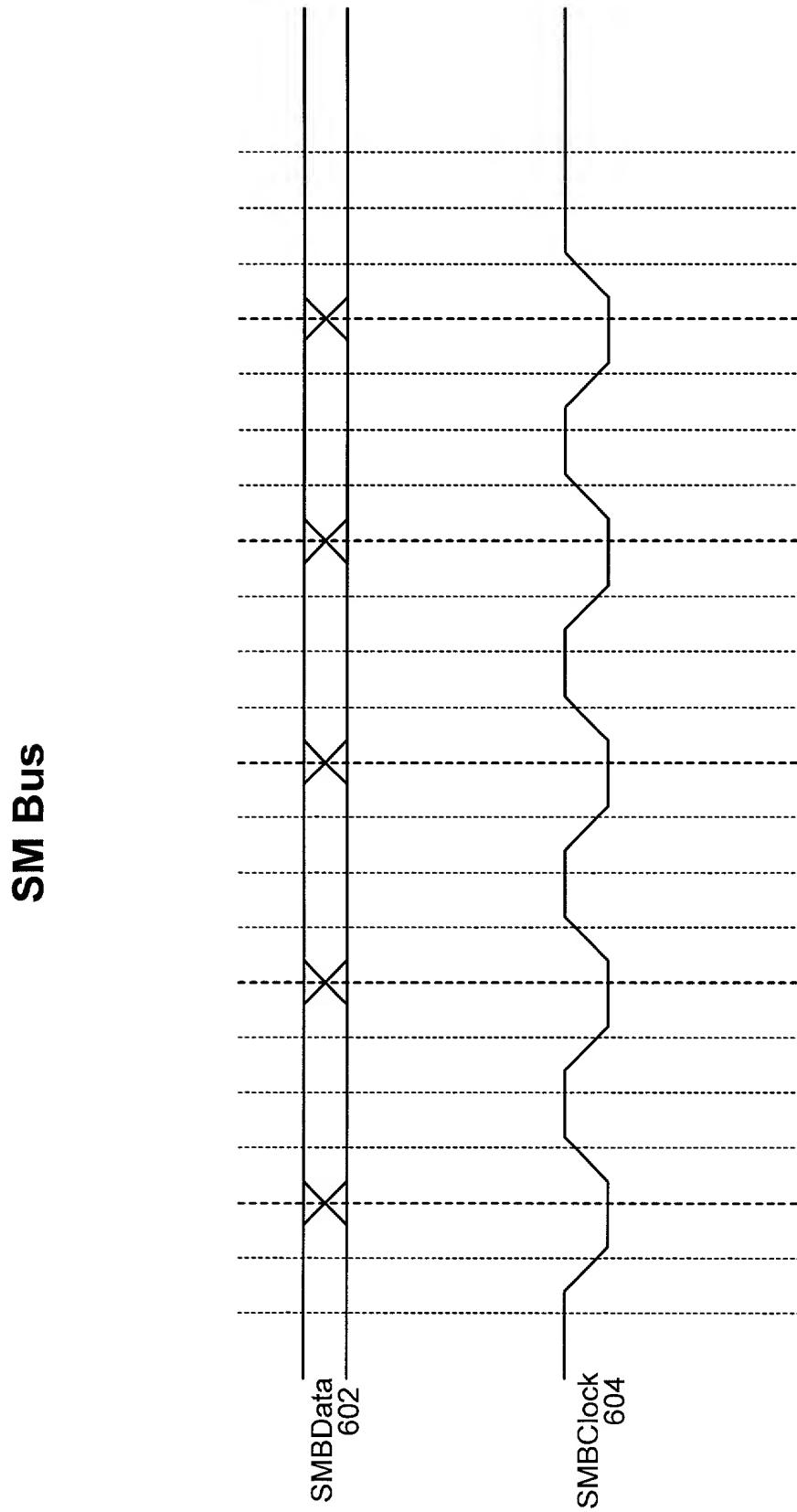


Fig. 5

Fig. 6
Prior Art



Command Byte

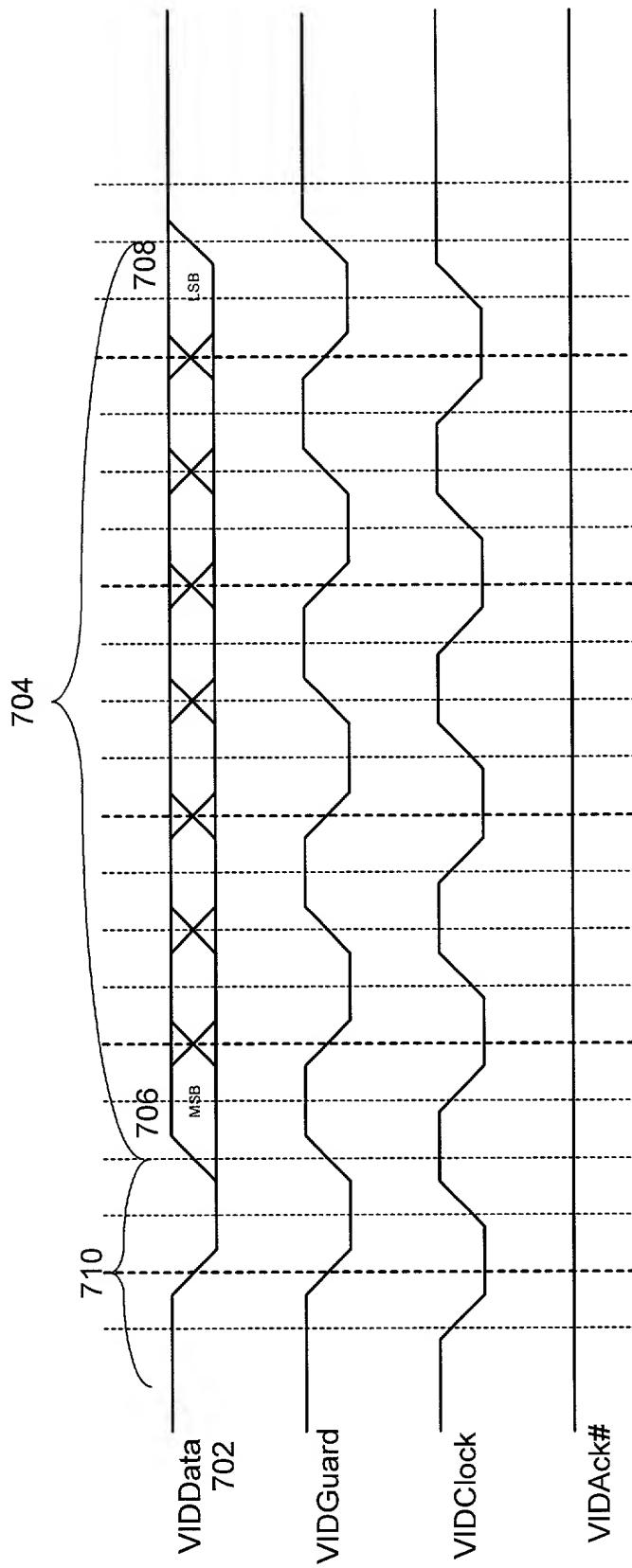


Fig. 7

Data Out Byte

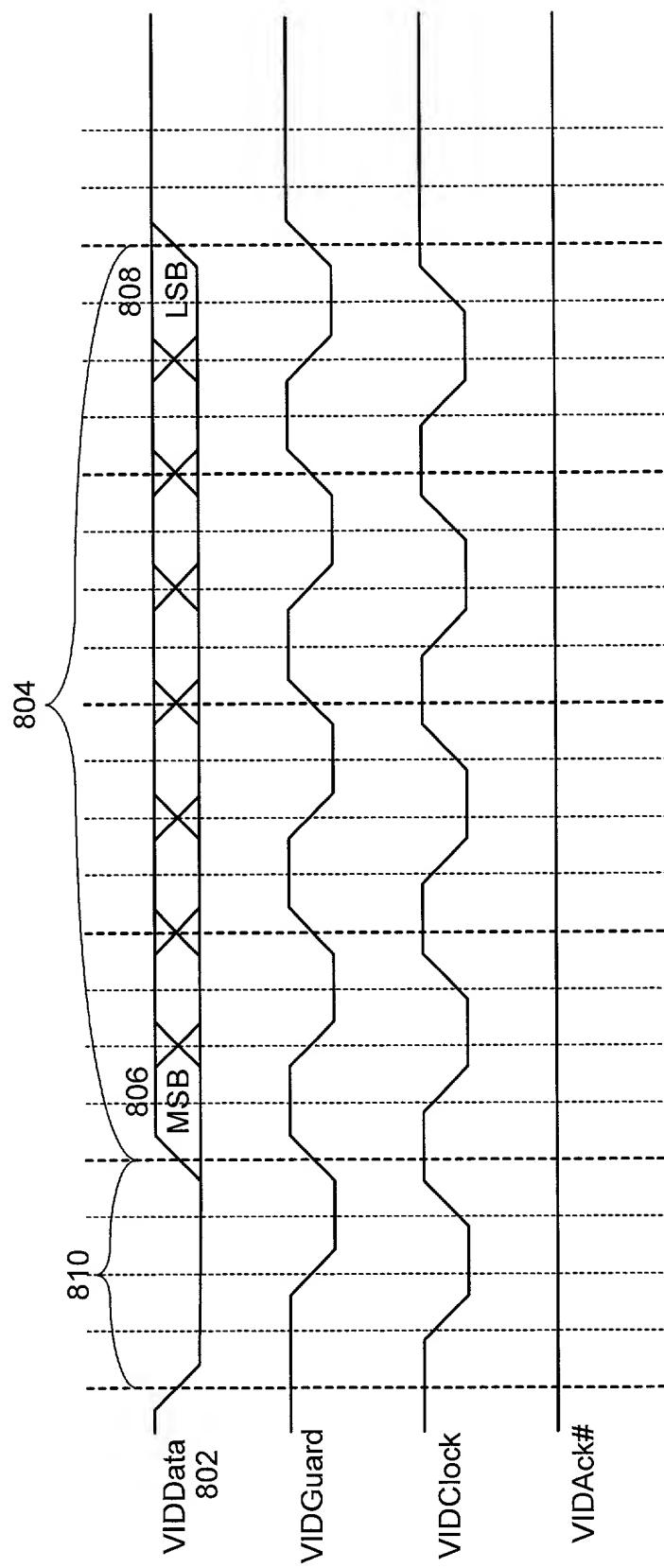


Fig. 8

CRC-8 Byte

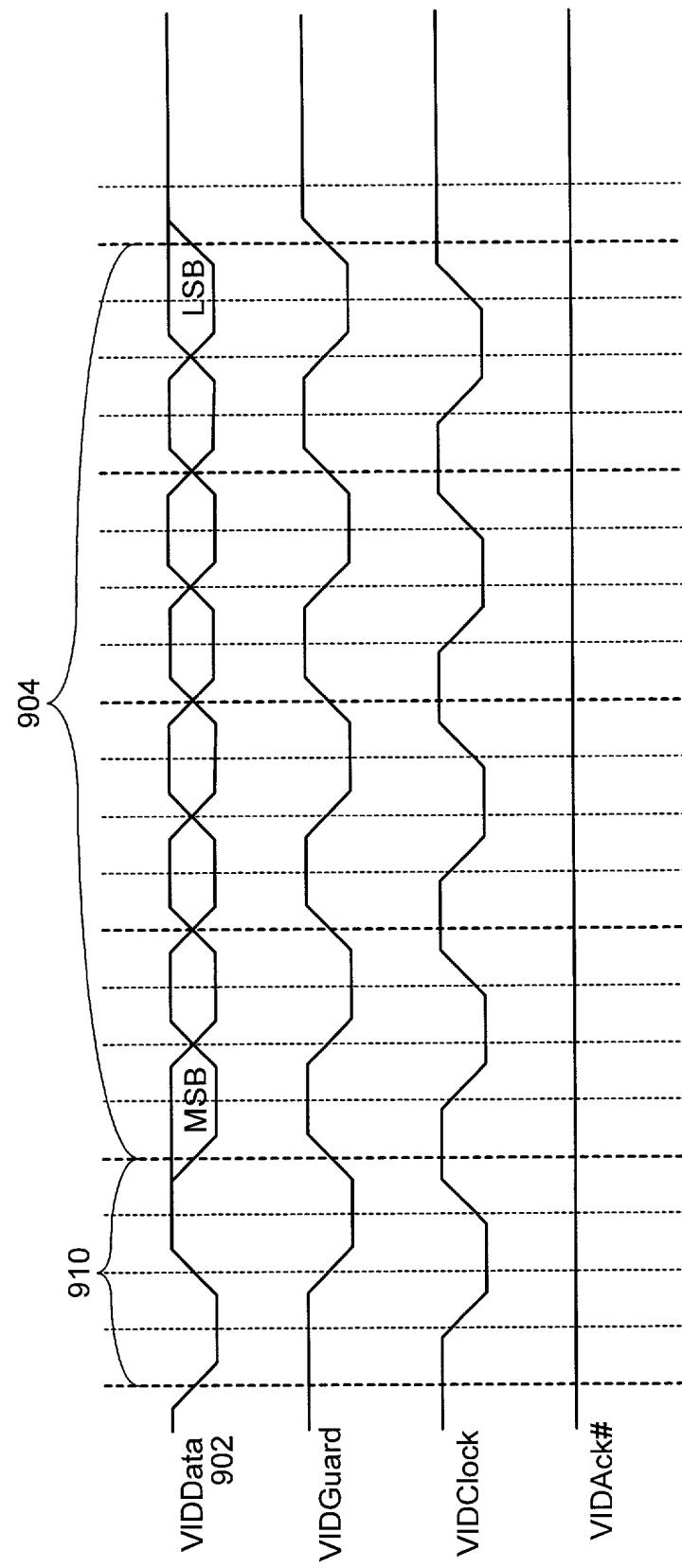


Fig. 9

Ack Byte with Positive Acknowledgement

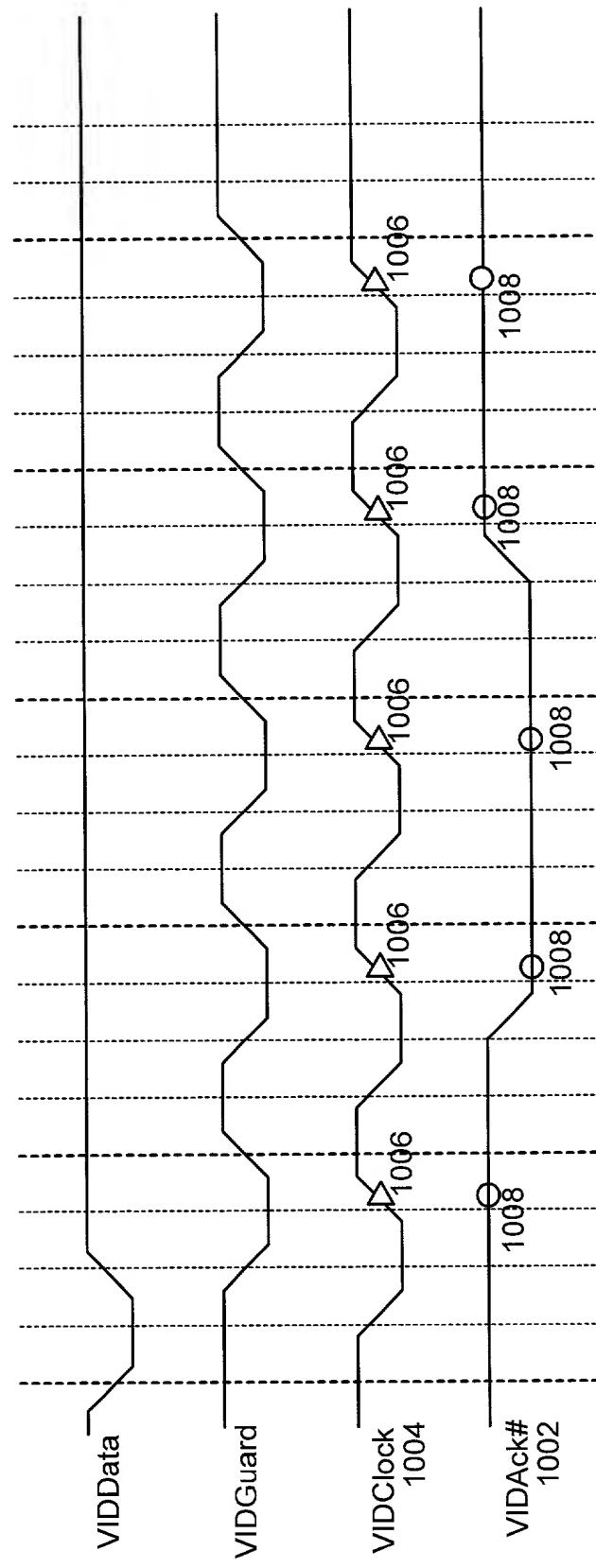


Fig. 10

Sync Byte

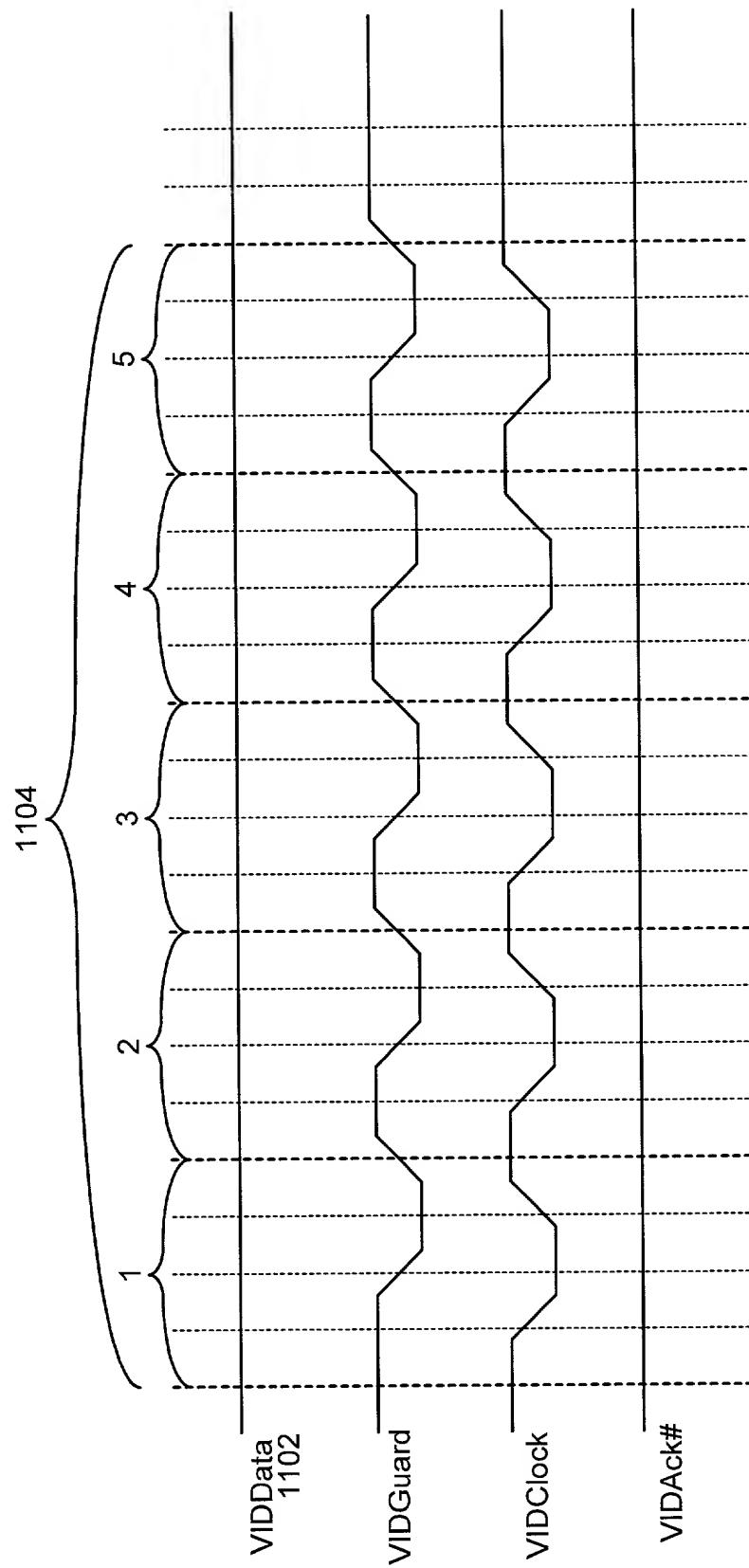


Fig. 11

Complete Command

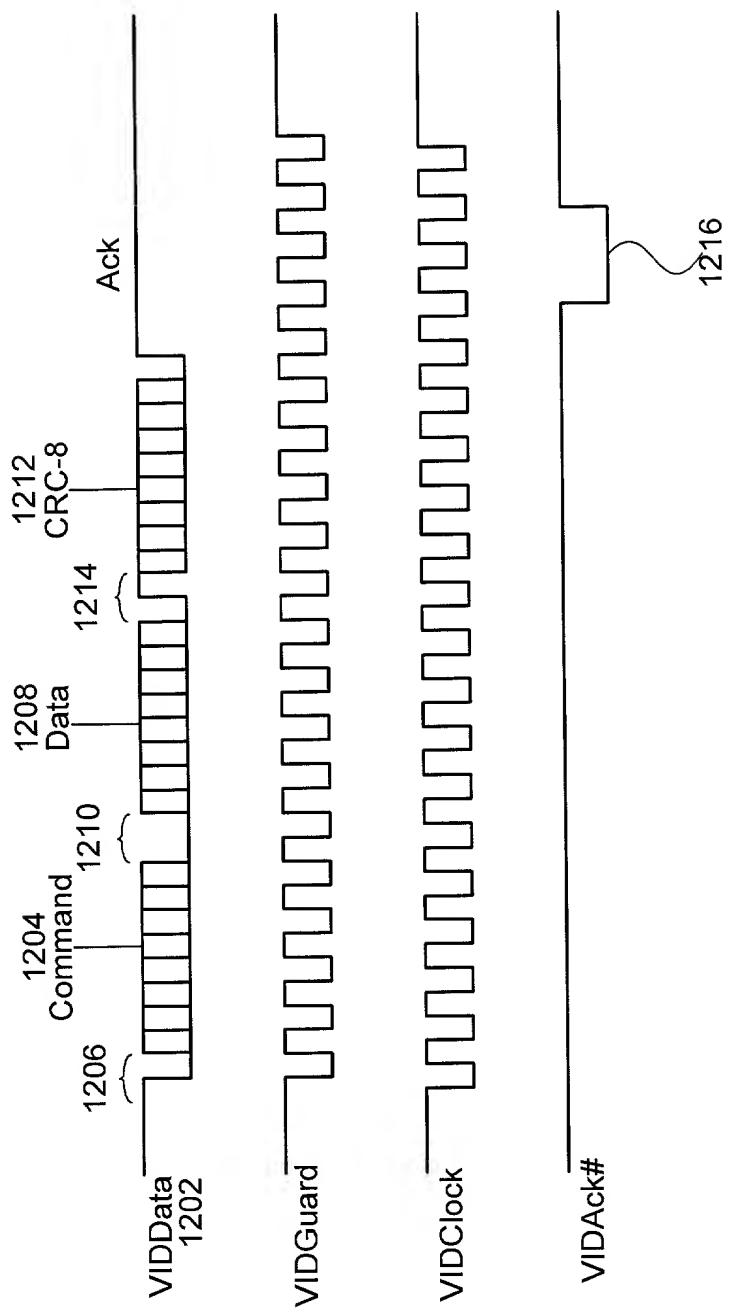


Fig. 12